## REMARKS/ARGUMENTS

Claims 1 and 3-10 remain in this application. Claims 1 and 3-10 have been amended. No Claims are added. Claims 2 and 11 are deleted because of the limitation “wherein said erase voltage between about 12 volts” is not described in the specification. Furthermore, in claims 5, the recitation “between about 12 volts” is deleted, and the erase voltage is applied to the “N-type well region”, not to “P-type drain”. Thus, Applicant also amended “P-type drain” with -- N-type well region --.

Applicant amended the entire specification for misspelling, and all possible minor errors in the specification have been amended. Applicants respectfully requests reconsideration in light of the following remarks.

## SPECIFICATION OBJECTION

With respect to Page 2 of the Office Action, the Examiner objected Specification.

Applicant corrected the all possible minor errors in the specification, for example: on page 3, line 21, the unnecessary word “ot” is deleted, and on page 8, line 19, the mistyped word “salient” is amended with -- silent --. Furthermore, Applicant amended the entire error in the specification, thus, the objection of the specification can be withdrawn.

## DRAWINGS OBJECTION

With respect to Page 2 of the Office Action, the Examiner objected drawings.

According to the page 3, line 6 of the specification, the reference number 20 is mistyped. Applicant corrected the reference number "20" with -- 110-- in the specification. Thus, drawing is not to be corrected, and the objection of drawings can be withdrawn.

## CLAIM REJECTIONS- 35 U.S.C. SECTION 112, second paragraph

Claims 4, 7-8, and 10-11 stand rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Applicant amended the vague and not clear recitation of Claim 7, "wherein said source line is divided along a bit direction by using an isolation structure" with -- wherein said source line is divided by an isolation structure along a bit line direction --, thus, Applicant believed the rejection of Claim 7 that can be traversed.

Applicant amended the limitation of claim 8, "a" with -- said --, to overcome the insufficient antecedent basis for the limitations of "a supply voltage". Further, in claim 5, the supply voltage is applied to said "control gate", not to the N-type well region", thus, Applicant corrected the recitation "N-type well region" with -- control gate – in Claim 8.

Applicant amended the vague and not clear recitation of Claim 10 "applying an erase voltage to said P-type drain region to cause tunneling of electrons from a floating to said N-type well region and to said N-type well region,..." with -- applying an erase voltage to said P-type drain region to cause tunneling oxide layer of electrons floats from a floating gate to said N-type well region, wherein said P-type drain region coupled to a bit line --. Thus, Applicant believed that the rejection of Claim 10 can be traversed. In addition, because of the rejection of Claim 10 is traversed according to the amendment, therefore, the rejection of Claim 11 is also traversed.

## CLAIM REJECTIONS- 35 U.S.C. SECTION 112, first paragraph

Claims 2, 5, 9, and 11 stand rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such as way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The recitation of Claims 2, 5, and 11 "wherein said erase voltage between about 12 volts" does not described in the specification, thus, Applicant deleted the claims 2 and 11 to overcome the rejection of 35 U.S.C. 112, first paragraph. In addition, in Claim 5, the recitation "between about 12 volts" is deleted, and the erase voltage is applied to the "N-type well region", not to "P-type drain". Therefore, Applicant believed that the rejection of above claims is traversed.

With regards to Claim 9, the limitation of "wherein said cell programmed by applying a negative supply voltage between 6-10 to said P-type drain region" is not described in the specification. According to the specification, on page 12, lines 4-6 "the non-volatile memory cell is programmed by applying a negative voltage around -4 t -6 volts to the drain region to induce hot electrons". Thus, the limitation of "wherein said cell programmed by applying a negative supply voltage between 6-10 to said P-type drain region" is amended with -- wherein said cell programmed by applying a negative supply voltage between -6 to -10 volts to said P-type drain region". In addition, according to the specification, on page 12, lines 22-23 "wherein the threshold voltage Vt in the preferred embodiment is around -4 volts". Thus, the limitation of "a negative threshold voltage is of about 2 volts applied to said word line" of claim 9 is amended with – a negative threshold voltage is of about -4 volts applied to said word line--.

## CLAIM REJECTION-35 U.S.C SECTION 102 (b)

Claims 1-11 stand rejected under 35 U.S.C. 102(b) as being anticipated by Onakado et al (U.S. Patent No. 5,818,761).

Claims 2 and 11 have been deleted, thus, the rejection for claim 2 and 11 are not existence.

Respect with Onakado et al '761, which discloses "in the erasing operation, a negative potential of about -5 to -12V is applied to 'control gate electrode', a positive potential of about +5 to about +12V is applied to source impurity region and N well, and drain impurity region is set to open state (col. 5, lines 12-16).

Regards as Amended Claims 1, 5, and 10, recited "wherein said non-volatile memory cell is erased by applying an erase voltage to said 'P-type drain region', applying a supplying voltage to said control gate, and said erase voltage applied to said N-type well region.". The voltage is applied to different region that would be induced the different operating result. In the disclosure of Onakado et al '761 which disclosed **"a negative potential of about -5 to -12V is applied to 'control gate electrode"** and **"a positive potential of about +5 to**

**about +12V is applied to source impurity region and N well**". Nevertheless, the present invention recited the **voltage is applied to the "P-type drain region", "said erase voltage applied to said N-type well region"**, and **there is no voltage potential is applied to the "source region"**. In the disclosure of Onakado et al '761 did not disclose the **voltage potential is applied to the "P-type drain region"** and **there is no voltage potential is applied to the "source region" during the erasing operation**.

In addition, Onakado et al '761 disclosed that the "a positive potential of about +5 to about +12V is applied to source impurity region and N well". Nevertheless, the present invention recited "the source line is coupled to the P-type drain region, **said source line exhibits floating** (as Claim 3 recited)". That is to say, **there is no voltage potential to the source line in the present invention**. Thus, in the disclosure of Onakado et al '761 disclosed the "a positive potential of about +5 to about +12V is applied to source impurity region and N well" is different from the present invention.

Moreover, Onakado et al '761 disclosed when electrons are injected to the floating gate electrode, the efficiency of ....by FN tunneling current used for programming or erasing operation (col. 5, lines 60-66). Nevertheless, regards as amended claim 10, Onakado et al '761 did not disclose the recitation of "applying an erase voltage to said P-type drain region to cause tunneling oxide layer of electrons floats from a floating gate to said N-type well region,..." as in amended claim 10. In the disclosure of Onakado et al '761, the "electrons are injected to the floating gate electrode" is different between the "electrons floats from a floating gate to the N-type well region" as claim 10 recited. Therefore, the electrons float into the different elements, the operation of the semiconductor device is also different between the

**"electrons injected to the floating gate"** and **"electrons float from a floating gate"**. Thus, Applicant believed Onakado et al '761 cannot anticipate the above claims, and the rejection of above claims can be traversed.

## Conclusion

In the light of the above amendments and remarks, Applicant respectfully submits that all pending Claims 1 and 3-10 as currently presented are in condition for allowance. Applicant has concluded that this reference does not affect the patentability of these claims as currently presented. Accordingly, reconsideration is respectfully requested.

Respectfully submitted,

Sam Huang
Registration No. 48,430

Customer No. 004372
ARENT FOX PLLC
1050 Connecticut Avenue, N.W.,
Suite 400
Washington, D.C. 20036-5339
Tel: (202) 857-6000
Fax: (202) 638-4810